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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/492,265	01/27/2000	Yi-Hsien Hao	34556/JFO/B600	9668

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EXAMINER	
PHILPOTT, JUSTIN M	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/492,265	HAO ET AL.	
	Examiner	Art Unit	
	Justin M. Philpott	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 29, 2005 has been entered.

Response to Arguments

2. Applicant's arguments filed March 29, 2005 have been fully considered but they are not persuasive.

Specifically, applicant argues (pages 18-24) that Muller and/or Steiner do not teach the newly added limitation of a "key to index a location within the Address Resolution Table" recited in the independent claims. However, such a limitation is taught by the newly cited art as discussed in the following office action. Thus, applicant's argument is moot.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,021,132 to Muller et al. in view of U.S. Patent No. 6,529,519 to Steiner et al., further in view of U.S. Patent No. 5,860,136 to Fenner.

Regarding claims 1, 8, 9, 11, 13, 15, 21, 28, 32-34, 40, 52 and 57, Muller teaches a memory structure (e.g. see FIG. 1 and col. 3, line 52 – col. 7, line 40) comprising an Address Resolution Table (e.g., address table stored in forwarding memory 113, see col. 4, lines 32-34) for resolving addresses in a packet-based network switch (101); and a Packet Storage Table (e.g., shared memory manager 220 locally storing pointers which point to buffers that contain packet data, see col. 6, lines 43-63) adapted to receive a packet for storage in the packet-based network switch and sharing a preselected portion of memory with the Address Resolution Table, wherein Address Resolution Table utilizes a preselected portion of memory comprising the forwarding and filtering database 140 (FIGS. 1 and 2). Furthermore, regarding claims 8, 13, 32, 52 and 57, Muller teaches the Address Resolution Table (113) has an associative memory structure (e.g., associative memory 114 within database 140 and further coupled to switch fabric 210). Still further, regarding claims 8, 9, 13 and 32, Muller teaches the Packet Storage Table is adapted to receive at least one of each of a Packet Data Address (e.g., within the header received from forwarding decision, see col. 5, line 46 – col. 6, line 40) and a Packet Data Value (e.g., a priority indication, see col. 6, line 21). Additionally, regarding claims 11, 33, 52 and 57, Muller teaches the associative memory structure (114) is a direct-mapped/one-way associative memory structure, such that the associative memory structure (114) stores data associated with each entry in the Address Resolution Table (113) (e.g., see col. 4, lines 30-37).

However, Muller may not specifically disclose a single buffer per packet mechanism or an index key.

Steiner also teaches a memory structure for buffering packets. More specifically, Steiner teaches an improvement for packet buffering wherein a single buffer per packet mechanism (e.g., single "page" buffer per packet, see col. 5, lines 54-65 and col. 7, lines 55-62) is configured to receive an individual packet for enabling only one transmit descriptor (e.g., one pointer in table of pointers, see col. 5, lines 54-65 and col. 7, line 63 – col. 8, line 3 regarding addresses) read per the individual packet and to enable an execution of a single access in order to locate an entire packet to be transmitted (e.g., see col. 5, lines 54-58 wherein each page comprises a single packet, and see col. 7, line 63 – col. 8, line 3 wherein an access of an address of a page therefore enables location of an entire packet). The teachings of Steiner resolve the memory fragmentation problem of gaps (e.g., see col. 2, lines 37-45) while conserving processor resources (e.g., see col. 2, line 46 – col. 3, line 10), yielding a buffer with reduced processor loading and increased power-conservation (e.g., see col. 3, line 11 – col. 4, line 15). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the teachings of Steiner to the system of Muller in order to provide buffering with reduced processor loading and increased power-conservation.

However, Muller in view of Steiner may not specifically disclose an index key.

Fenner also teaches a memory structure (e.g., memory, see col. 6, lines 18-63, and particularly line 39), and specifically, teaches using a key (e.g., key, see col. 6, lines 34-53) to index a location within an address table (e.g., via index table, see col. 6, lines 34-53), wherein a packet can be located using the key (e.g., stored records of packet data, see col. 6, lines 34-53

and col. 1, lines 50-60). Additionally, the teachings of Fenner also provide increased speed of operation with greater system adaptability and reduced cost (e.g., see col. 4, line 39 – col. 6, line 63, particularly col. 5, lines 40-63). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the memory structure teachings of Fenner to the memory structure of Muller in view of Steiner in order to provide increased speed of operation with greater system adaptability and reduced cost.

Regarding claims 2, 18 and 37, Muller further teaches the structure comprises a Transmit Descriptor Table (e.g., output queue, see col. 7, lines 20-25) being associated with a corresponding packet-based network transmit port (output port 206); and a Free Buffer Pool (e.g., shared memory 230 comprising free pool of buffers, see col. 7, lines 25-67) having plural memory buffers each having a pre-determined number of memory locations (e.g., memory lines) associated therewith (e.g., see col. 8, lines 37-51).

Regarding claims 3, 29, 47 and 59, Muller teaches the structure implements an IEEE Standard 802.3 communication protocol (e.g., see col. 3, lines 57-62).

Regarding claims 4, 30, 48, 53 and 60, Muller teaches the switch comprises plural ports (e.g., see FIG. 2 input and output ports 206).

Regarding claims 5, 49, 50, 54 and 55, Muller in view of Steiner teach the structure discussed above regarding claims 4, 47 and 52, however, may not specifically require that the switch comprise at least 4 ports or at least 8 ports. However, Muller further teaches a plurality of ports are included (e.g., see FIG. 2), and Muller does not limit the scope of the invention to a specific number of ports. Thus, the teachings of Muller clearly encompass the limitations of providing at least 4 ports or at least 8 ports. Moreover, it is generally considered to be within the

ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to have the switch comprise at least 4 ports or at least 8 ports since the teachings of Muller clearly encompass the limitations of providing at least 4 ports or at least 8 ports and since it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value

Regarding claims 6, 14 and 58, Muller teaches the associative memory comprises a search structure (e.g., search engine within coupled switch fabric block 210, see col. 6, lines 4-7).

Regarding claims 7, 12, 22, 31, 41, 51 and 56, Muller in view of Steiner teach the structure discussed above regarding claims 3, 11, 21, 28, 34, 45 and 52, however, may not specifically disclose a specific number of memory accesses required per Ethernet frame. However, Regarding claims 7, 12, 22, 31, 41, 51 and 56, these claims were rejected in a previous office action by the Examiner taking official notice that the limitations recited in these claims are well known in the art. That is, it is commonly known in the art to perform, e.g., one cycle per Ethernet frame for operations such as address resolution/learning and transmission read/write. In Applicant's response to the previous office action, Applicant has not traversed the Examiner's

assertion of official notice or Applicant's traverse is not adequate. Therefore, in accordance with MPEP 2144.03(C), the limitations recited in these claims comprise well-known art and are hereafter taken to be admitted prior art.

Regarding claim 10, as discussed above regarding claims 2, 18 and 37, Muller in view of Steiner teach the structure comprises a Transmit Descriptor Table (e.g., output queue, see col. 7, lines 20-25 of Muller) being associated with a corresponding packet-based network transmit port (output port 206); and a Free Buffer Pool (e.g., shared memory 230 comprising free pool of buffers, see col. 7, lines 25-67) having plural memory buffers each having a pre-determined number of memory locations (e.g., memory lines) associated therewith (e.g., see col. 8, lines 37-51). However, Muller in view of Steiner may not specifically disclose receiving a Table Descriptor Address and a Table Descriptor Value at the Transmit Descriptor Table. Nevertheless, Muller clearly suggests that the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value by way of previous example, wherein Muller teaches Address and Value are received by the Packet Storage Table as discussed above regarding claims 8, 9, 13 and 32, and wherein Muller further teaches in steps (1) – (5) (see col. 5, lines 46-65) processing packets from Address Resolution Table (113) to Packet Storage Table (220) to Free Buffer Pool (230) and finally to Transmit Descriptor Table (at output queue 206), thus, clearly suggesting that Address and Value are also received by the Transmit Descriptor Table. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to adapt the Transmit Descriptor Table of Muller in view of Steiner to receive a Table Descriptor Address and a Table Descriptor Value as suggested by Muller by teaching adapting the Packet Storage Table to receive an Address and Value and further teaching steps (1) – (5)

wherein packets are processed from Packet Storage Table to Free Buffer Pool and finally to Transmit Descriptor Table.

Regarding claims 16, 17, 35 and 36, Muller in view of Steiner teach the structure discussed above regarding claims 13 and 32, however, may not specifically require that the Transmit Descriptor Table (output queue) comprise a circular FIFO memory structure with head and tail pointers. However, Muller clearly teaches performing output queuing (output queues at output ports 206), and further, claims 16, 17, 35 and 36 were rejected in the previous office action by the Examiner taking official notice that the limitations recited in these claims are well known in the art. That is, a circular FIFO memory structure with head and tail pointers is well known in the art for implementing suitable output queuing. In Applicant's response to a previous office action, Applicant has not traversed the Examiner's assertion of official notice or Applicant's traverse is not adequate. Therefore, in accordance with MPEP 2144.03(C), the limitations recited in these claims comprise well-known art and are hereafter taken to be admitted prior art.

Regarding claims 19, 20, 38 and 39, Muller teaches the Free Buffer Pool further comprises a buffer control memory (e.g., tag array, see col. 9, line 57 – col. 10, line 45) comprising plural memory bits (e.g., represented by rows and columns) uniquely corresponding to ones of the pre-determined number of buffer pool memory locations.

Regarding claims 23 and 42, Muller teaches the structure further comprises a free buffer manager (e.g., shared memory manager comprising buffer tracking unit 329 and coupled with switch fabric 210, see FIGS. 2, 3B and 4) including: a buffer bus controller (e.g., buffer manager 325, see col. 9, line 5 – col. 14, line 37), a buffer bus register (e.g., arbitor 470), a buffer control

finite state machine (e.g., array controller 450) operably coupled with the bus controller and the bus register, and a buffer search engine (e.g., search engine within block 210, see col. 6, lines 1-23) operably coupled with the bus controller, bus register, and finite state machine.

Regarding claims 24 and 43, Muller teaches the buffer bus controller comprises a buffer free bus controller (performed by buffer manager 325) for detecting a buffer request (Br_Ptr_IP-Bus Request) and presenting the request to at least one of the finite state machine and the buffer search engine (e.g., see col. 13, lines 5-14), and a buffer grant bus controller (performed by buffer manager 325) for granting an available free buffer (Br_Ptr_Data_BM_to_IP[X:0]) as indicated by the buffer bus register (e.g., see col. 13, lines 15-23).

Regarding claims 25 and 44, Muller teaches the buffer search engine comprises a pipelined buffer search engine by coupling learning logic (e.g., see col. 6, line 5) to the search engine for searching and maintaining the database 140.

Regarding claims 26, 27, 45 and 46, Muller in view of Steiner teach the structure discussed above regarding claims 23 and 42, however, may not specifically require that the buffer bus register comprise an eight-location LIFO. However, Muller clearly teaches performing queuing (output queues at output ports 206), and further, claims 26, 27, 45 and 46 were rejected in a previous office action by the Examiner taking official notice that the limitations recited in these claims are well known in the art. That is, LIFO is a queuing technique well known in the art. In Applicant's response to the previous office action, Applicant has not traversed the Examiner's assertion of official notice or Applicant's traverse is not adequate. Therefore, in accordance with MPEP 2144.03(C), the limitations recited in these claims comprise well-known art and are hereafter taken to be admitted prior art.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent No. 5,930,359 to Kempke et al. also discloses an addressable memory which utilizes an index key.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M. Philpott whose telephone number is 571.272.3162. The examiner can normally be reached on M-F, 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on 571.272.3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin M Philpott

ALPUS H. HSU
PRIMARY EXAMINER